**WHAT IS CLAIMED IS:**

1. A clock lock detection circuit comprising:

a first input indicating an edge of a first clock;

a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference;

a difference generation module for generating a difference signal based on the time difference between the first and second inputs; and

a voltage divider module for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs.

2. The circuit of claim 1 wherein the voltage divider module has a CMOS inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

3. The circuit of claim 1 wherein the difference generation module is an XOR gate.

4. The circuit of claim 1 further comprising a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for

generating a lock signal indicating whether the time difference is within the allowable time difference.

5. The circuit of claim 4 wherein the voltage comparator is a Schmitt trigger.

6. The circuit of claim 4 further comprising a buffer module passing the lock signal.

7. A clock lock detection circuit comprising:

a first input indicating an edge of a first clock;

a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference;

a difference generation module for generating a difference signal based on the time difference between the first and second inputs;

a voltage divider module containing a capacitor for receiving the difference signal and generating an indication voltage which varies due to a charging and discharging process of the capacitor influenced by a change of the time difference between the first and second inputs; and

a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference is within the allowable time difference.

8. The circuit of claim 7 wherein the voltage divider module has a CMOS inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

9. The circuit of claim 7 wherein the difference generation module is an XOR gate.

10. The circuit of claim 7 wherein the voltage comparator is a Schmitt trigger.

11. The circuit of claim 7 further comprising a buffer module passing the lock signal.

12. A method for detecting whether two clock signals have an allowable time difference, the method comprising:

generating a first signal indicating an edge of a first clock;

generating a second signal indicating a corresponding edge of a second clock wherein the edge of the second clock is expected to be close to the edge of the first clock within the allowable time difference;

generating a difference signal based on a time difference between the first and second signals; and

generating an indication voltage which varies based on a change of the time difference between the first and second signals.

13. The method of claim 12 wherein the generating an indication voltage further includes feeding the difference signal into a voltage divider module having a CMOS inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter and, wherein the indication voltage is the output of the CMOS inverter.

14. The method of claim 12 wherein the generating of a difference signal further includes feeding the first and second signals to an XOR gate for generating the difference signal.

15. The method of claim 12 further comprising comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference between the first and second signals is within the allowable time difference.

16. The circuit of claim 12 wherein the voltage comparator is a Schmitt trigger.

17. The circuit of claim 12 further comprising a buffer module passing the lock signal.

18. A phase lock loop circuit comprising:

a first flip-flop receiving a first clock and generating a first signal indicating an edge of the first clock;

a second flip-flop receiving a second clock and generating a second signal indicating a corresponding edge of the second clock wherein the edge of the second clock is expected to be close to the edge of the first clock within an allowable time difference;

a reset signal generator using the first and second signals to generate a reset signal for the first and second flip-flops;

a clock lock detection circuit comprising:

a difference generation module for generating a difference signal based on the time difference between the first and second signals;

a voltage divider module containing a capacitor for receiving the difference signal and generating an indication voltage which varies due to a charging and discharging process of the capacitor influenced by a change of the time difference between the first and second signals; and

a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference is within the allowable time difference.

19. The circuit of claim 18 wherein the voltage divider module has a CMOS inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

20. The circuit of claim 18 wherein the difference generation module is an XOR gate.